REMARKS

Claims 1-17 are currently pending in connection with the present application. Claims 1, 12, and 15 are independent claims.

Example Embodiment of the Present Invention

Figure 4 illustrates an example embodiment that reduces the area consumed by the chip package by connecting the input/output terminal to the substrate 303 directly underneath the chip 322, instead of in the peripheral region of the substrate as shown in the prior art, figure 2. The position of the connection terminals' position underneath the chip may increase the usable mounting area on the motherboard, as the area consumed by the package is considerably reduced, as compared to the prior art package in figure 2.

Example embodiments may also reduce the height of the overall package by reducing the height of the connections used to connect multiple chip packages, by not relying on solder balls to electronically interconnect the chip packages.

The example embodiment in figure 4 shows two chip packages 320A and 320B, connected using an adhesive layer 309, and electrically connected using flexible cable 306, to the lower substrate surface 303 of the chip package, using wired connections 322. Conventional solder balls 307 allow the entire package to be connected to a motherboard. Figure 5A shows the lower surface of the substrate including bond wire connections 304 which connect to wires 322 (from figure 4). Connecting pads 311A connect to the flexible cable 306, allowing the upper chips to connect to the lower chip via the lower chip's lower substrate. By removing an exposed interconnection (gap between the packages in figure 3, 703) between the surface packages, the overall height of the entire package maybe reduced. Furthermore, by allowing interconnection

below the chip (in contrast to figure 2) the area consumed by the chip package maybe limited to the area of the semiconductor chip.

At least one embodiment of the present invention provides for a stack of area array type packages, such as ball grid array (BGA) packages, that may reduce the interconnection paths from each package to the external connection terminals. Example embodiments may reduce the height of the overall stacked chip package or increase the usable density on the main board.

§103(a) Corisis/Cady Rejection

Claims 1-3, 7, and 9-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis et al. (U.S. PG Pub. 2001/0040282), in view of Cady et al. (U.S. Patent No. 6,576,992). Applicant respectfully traverses this rejection.

Corisis teaches a stackable ball grid array package. Each chip package includes a chip 14, connected to an attach pad 16, a substrate 12, solder balls 28, and wire bonds 22 used to connect the chip to the substrate. The chip packages are attached to each other via solder balls 28 located towards the outer periphery of the package (P in figure 1), and not in overlapping proximity to the chip. Corisis teaches that as the chips and grid array densities increase, the desire in packaging semiconductor chips has been to reduce the overall height of the semiconductor package (paragraph 0004). Corisis also teaches that wires on the outer edges of the semiconductor chip add harmful inductance and unnecessary signal delay (paragraph 0007). The circuit path leading from each chip to the consecutive chip follows from the first chip 14, to the first bond wires 22, to a first substrate 12, through the solder balls 28, to the second substrate 12, and through the second bond wires 22 to the second chip 12. Alternatively, for chip stacks containing more than 2 chips (i.e. figure 1), the substrates possess isolated conductive elements

29 and 31 (figure 9) located on the substrate that allow signals to pass through the second substrate to a third, fourth, fifth ... or nth substrate via a plurality of solder ball and substrate layers.

On page 3 of the Office Action, the Examiner acknowledges that Corisis is silent with regards to having:

> at least one flexible cable having a plurality of conductive patterns thereon extending around at least one side edge of a lower one of the at least two packages, and electrically coupling the connecting pads of the packages through the conductive patterns

as recited in claim 1, and "a non-conductive adhesive layer interposed between adjacent lower and upper packages" as recited in claim 13.

Cady teaches the stacking of chip scale-packaged integrated circuits. The chip packages, 12 and 14, are stacked in an overlapping fashion, connected by a flexible circuit structures, 30 and 32, wrapped about the lower packages and attached to the next highest chip via solder balls 24. The circuit path leading from each chip to the consecutive chip follows from the first chip 12 to a first set of solder balls 24 attached to flexible circuits 30 and 32, through a second set of solder balls 24, to the second chip 14.

Lack of Motivation to Combine References

Applicant submits that the Examiner has not supplied evidence of the motivation necessary to lead one of ordinary skill in the art to combine the teachings of Corisis et al. and Cady et al. Accordingly, absent such motivation, a prima facie case of obviousness under 35 U.S.C. §103(a) has not been established and the rejection must be withdrawn.

Applicant directs the Examiner's attention to two recent cases decided by the Court of Appeals for the Federal Circuit (CAFC), In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed.Cir. 1999) and In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed.Cir. 2000). Both of these cases set forth very rigorous requirements for establishing a prima facie case of obviousness under 35 U.S.C. §103(a). To establish obviousness based on a combination of elements disclosed in the prior art, there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the Applicants. The motivation suggestion or teaching may come explicitly from one of the following:

(a) the statements in the prior art

(b) the knowledge of one of ordinary skill art, or

(c) in some cases, the nature of the problem to be solved.

See Dembiczak 50 USPQ at 1614 (Fed.Cir. 1999).

In order to establish a prima facie case of obviousness under 35 U.S.C. §103(a), the Examiner must provide particular findings as to why the two pieces of prior art are combinable. See Dembiczak 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence".

The alleged motivation for combining Corisis and Cady to reject amended independent claims 1, 12 and 15, asserted by the Examiner, is: "to make a compact stacked package for high-density modules."

Applicant asserts that the motivation alleged by the Examiner is based upon applicant's invention and is therefore improper hindsight. The Examiner has viewed the present application and selected prior art relating to "stacking semiconductor chips" without identifying or discussing any specific evidence of motivation to combine the references, other than providing

conclusory statements regarding the motivation and obviousness. Neither Corisis, nor Cady suggest combining the elements necessary to teach all the features of either independent claim 1, 12 or 15, nor has the Examiner cited any particular passage of Corisis or Cady, or provided evidence that such a combination would be obvious to one of ordinary skill in the art.

On the contrary, the disclosed references do not constitute an obvious combination because they seek to overcome different problems associated with stacking chip packages and teach away from each other.

Corisis teaches that as the chips and grid array densities increase, the desire in packaging semiconductor chips has been to reduce the overall height or profile of the semiconductor package (paragraph 0004). Corisis, in paragraph 0007, teaches away from assemblies that require wires or circuitry on the outer edges of the semiconductor chip, because these connections add harmful inductance and unnecessary signal delay. Furthermore, this will extend the profile beyond to the outer periphery of the lead wires reaching from the chip to the outer edges. In paragraph 0009, Corisis discloses that the FBGA package is configured such that conductive elements are placed along the outside perimeter of a semiconductor device, and that the conductive elements (e.g. solder balls) must only extend from the bottom and top surface of the IC device. Corisis solves the inner connection chip packages problem between the separate chips by using isolated conductive elements such as 29 and 31, in figure 9, to allow interconnection among other packages stacked on top of the other within the stacked package arrangements.

Cady seeks to solve the problem of stackable chip packages by reducing the area used on the motherboard without increasing the area consumed by the stacked chip packages as taught in Corisis (Column 1, lines 48-53). Cady employs a pair of flex circuits partially wrapped about the

outer edges of the lower CSP of the module. The flex circuit pair connects the upper and lower CSP and provides the thermal and electric path connection between the separate packages.

This clearly conflicts with Corisis' goal of avoiding the use of lead wires which can potentially adds harmful inductance and unnecessary signal delay and form the weak link in the connection between the semiconductor device packages.

Accordingly, Corisis and Cady cannot be combined to teach or suggest the features of claims 1. Therefore, claim 1 is patentable. Claim 12, and 15, are also patentable, at least for the reasons set forth above in regards to claim 1. Furthermore, claims 2-11, 13, 14, 16, and 17, are also allowable, at least because they depend on patentable claims 1 and 12.

Therefore, withdrawal of the rejection is respectfully requested.

The disclosed combination fails to meet the claimed features

Applicant submits that even if Corisis could be combined with Cady (which applicant does not admit for the reasons set forth above), the combination still fails to meet all the features of claims 3 and 12.

An example embodiment of the present invention disclosed in paragraphs 0030 and 0031 of the specification, teaches that terminal pads 311a may be connected to the semiconductor chip 301 through the first conductive pattern 313a, and the connecting pads 314a may be connected to the semiconductor chip 301 via the terminal pads 314a and first conductive pattern 313a. In the Example Embodiment the semiconductor chip 301 is not connected to the terminal pads, but instead may connect to the 'other end' of the first conductive pattern 313a by the bonding wires 304, as shown in figure 5a.

Claims 3 states "wherein **the substrate further has** first wiring providing electrical paths coupling the semiconductor chip and the terminal pads and second wirings providing electrical paths coupling chip and the connecting pads."

Corisis discloses that the semiconductor chip 14 connects to the terminal pads 20 via bonding wires 22 (figure 9). Cady discloses that the semiconductor chips 12/14 are connected via solder balls 24 to a flexible circuit 30/32. Cady does not disclose **a substrate** with either connecting pads or terminal pads. Accordingly, the combination of Corisis and Cady cannot teach the feature of claim 3 recited above.

In view of the above remarks, applicant submits that claim 3 is allowable at least for the reasons set forth. Claim 12 is also allowable as least for the reasons set forth above. Furthermore, claims 13, 14, 16 and 17 are allowable at least because they depend on allowable claims 3 and 12.

Therefore, withdrawal of the outstanding rejections in respectfully requested.

§103(a) Corisis/Cady/Kim Rejection

Claims 4-6, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis and Cady, further in view of Kim et al. (U.S. PG Pub. 2002/0043702). Applicant respectfully traverses this rejection.

The Examiner admits that Corisis and Cady does not teach "wherein the semiconductor chip is an edge pad type chip" as recited in applicant's claim 4.

Applicant submits that claims 4-6, and 17 are allowable because they depend on allowed amended independent claim 1, respectively, and Kim fails to make up for the deficiency

cussed above with respect to Corisis and Cady. Therefore, applicant respectfully requests that the outstanding rejection be withdrawn.

§103(a) Corisis/Cady/Rolda Rejection

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis and Cady, further in view of Rolda et al (US PG Pub. 2002/0030261). Applicant respectfully traverses this rejection.

The Examiner admits that Corisis and Cady does not teach "wherein the connecting pads are arranged in a staggered row near an edge of the substrate" as recited in applicant's claim 8.

Applicant submits that claim 8 is allowable because it depends on allowed amended independent claim 1, respectively, and Rolda fails to make up for the deficiency discussed above with respect to Corisis and Cady. Therefore, applicant respectfully requests that the outstanding rejection be withdrawn.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-17 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any

additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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